SIGNATURE ANALYZER OF BUILT-IN SELF TEST FOR ANALYZING STUCK-AT-FAULTS IN COMBINATIONAL LOGIC ICS

Widianto\textsuperscript{1}, Robert Lis\textsuperscript{2}
\textsuperscript{1}University of Muhammadiyah Malang, Indonesia
\textsuperscript{2}Wroclaw University of Science and Technology, Poland

Contact Person:
Widianto
Jl. Raya Tiogomas No. 246 Malang, Telp. +62341 464318
E-mail: widianto@umm.ac.id

Abstract

A signature analyzer of a built-in self test circuit is proposed to analyze stuck-at-faults occurring at input and output gates inside a combinational logic IC (Integrated Circuit). There are two types of the faults, namely stuck-at-1 and stuck-at-0. Logic values of the gate may be 1 and 0 values caused by stuck-at-1 and stuck-at-0, respectively. The test circuit consist of a pattern generator, multiplexers, demultiplexers, and the signature analyzer. In this paper, a feasibility of the test circuit is simulated using a Modelsim simulator. The IC of XXX0832 distributed by Nexperia Co.Ltd is used as a CUT (Circuit Under Test). Simulation results show that the faults inside it may be analyzed to be detected.

Keywords: signature analyzer, built-in self test, stuck-at-faults, combinational logic ICs

1. Introduction

A combinational logic IC (Integrated Circuit) is made by logic gates -AND, OR, NAND, NOR, INVERTER- connected or combined together for a specific function\cite{1,2}. An imperfect manufacturing process of the IC may input and output the gates occurred by stuck-at-faults\cite{3,4}. The function of the IC may be an error caused by the faults\cite{5}. Thus, they should be detected earlier before.

There are two types of the faults, i.e., a stuck-at-1 and a stuck-at-0\cite{6}. Logic values of input and output the gates may be 1 and 0 values caused by the stuck-at-1 and the stuck-at-0, respectively. For example, occurring stuck-at-0 at one of two inputs an AND gate may an output the gate always become an 0 value. However, the output gate always become an 1 value caused by occurring stuck-at-1 at it.

One the fault may be detected by a proposed BIST (Built-in Self Test) \cite{7}. However, it is difficult for applying it to the combinational logic IC, since many input and output gates inside it.

A BIST was proposed to detect the stuck-at-faults inside a combinational logic IC\cite{8}. Each response of the IC is provided by test vectors generated the BIST will be analyzed. It takes a long test time to detect the IC caused by the faults. Thus, the BIST should be revised.

In this paper, a BIST is added by a signature analyzer. The signature of the BIST is proposed to analyze stuck-at-faults occurring at input and output gates inside a combinational logic IC. A simulation circuit is designed and simulated by Verilog \cite{9,10} and Modelsim simulator, respectively. Simulation results show the stuck-at-faults may be analyzed to detect the faults faster than \cite{8}.

2. Research Method

A proposed BIST (Built-in Self Test) circuit is shown in Figure 1. The circuit consists of a PG (Pattern Generator), SAs (Signature Analyzers), Multiplexers, and De-multiplexers. An used CUT is a combinational logic gate.

The multiplexers and the de-multiplexers are two inputs-one input and one input-two outputs, respectively. Numbers of them are depend on numbers of inputs and outputs of the CUT. Both of them are controlled by a TMS (Test Mode Select). They are used to select the circuit works either in a normal mode or a test mode.

When an \textit{H} level signal is provided to the TMS, the circuit works in the normal mode. Signals provided to digital inputs, \textit{Di}0 to \textit{Din}, will be propagated to the CUT and outputted to digital outputs,
Do0 to Don. By providing an L level signal to the TMS, the circuit is in the test mode. The CUT will propagate signals generated by the PG. Then input them to the SA to be analyzed and observed by SA0 to SAn.

![Figure 1 BIST circuit](image1.png)

The PG circuit is made of D-FFs and an XOR gate as shown in Figure 2. Numbers of the D-FFs are based on input numbers of the CUT. Moreover, the PG is synchronized and initiated by clk and rst, respectively.

![Figure 2 PG circuit](image2.png)

Each SA circuit is made by D-FFs and two XOR gates as shown in Figure 3. Numbers of the D-FFs of the SA are equal numbers of the D-FFs of the PG. In addition, numbers of SAs are based on output numbers of the CUT. Also, clk and rst are used to synchronize and initialize the SAs, respectively.

![Figure 3 SA circuit](image3.png)

Input and output gates inside the CUT may be occurred by stuck-at-faults, a stuck-at-1 as well as a stuck-at-0. For instance, node e inside the CUT in Figure 4a occurred by the s-a-0, an output digital Do of the CUT become an L level logic signal regardless of logic signals in nodes a, b, and c. However, the Do in Figure 4b become an H level logic signal caused by the s-a-1 occurring at node e.

![Figure 4 Stuck-at-faults](image4.png)
3. Result and Discussion

Feasibility of a signature analyzer of a BIST circuit in which stuck-at-faults in a combinational logic IC may be analyzed is simulated by using Modelsim simulator. The simulation circuit is designed by Verilog and an XXX0835 from NXP SemiconductorCo.Ltd is used as a CUT. The circuit is shown in Figure 5. A node $e$ of the CUT is a targeted fault of a stuck-at-0.

The circuit works in two modes, i.e., a normal and a test modes. In order to work in the normal mode, an $H$ level signal is provided to $TMS$, signals of digital inputs, $Di0$ to $Di2$, will be propagated to the CUT and outputted to a digital output $Do0$.

![Figure 5 Circuit simulation](image)

When the $TMS$ is changed by providing an $L$ level logic signal, the circuit works in the test mode. The CUT will propagate signals generated by $PG$ and output them to $SA$, $SA0$ to $SA2$. A simulation result of a defect-free circuit shown in Figure 6.

![Figure 6 Defect-free Circuit](image)

In the defect-free circuit result, for example at a simulation time 33 – 36 ns, an output node of the CUT $e = 1$. Since generated signals by $QPG$ of the SA are 100. It means that the signals are inputted to the CUT nodes $c$, $b$, and $a$, respectively. Thus, $c = 1$, $b = 0$, and $a = 0$. The simulation time result is shown in Figure 7.

```markdown
# T=33, QPG=011, QPGn=100, QSA=001, QSAN=110, rst=0, Di0 = 0, Di1 = 0, Di2 = 1, TMS = 0, e = 1, SA=1, Do0=0
# T=35, QPG=011, QPGn=100, QSA=001, QSAN=110, rst=0, Di0 = 0, Di1 = 1, Di2 = 1, TMS = 0, e = 1, SA=1, Do0=0
# T=36, QPG=011, QPGn=100, QSA=001, QSAN=110, rst=0, Di0 = 1, Di1 = 1, Di2 = 0, TMS = 0, e = 1, SA=1, Do0=0
```
Figure 7 Simulation time result of defect-free circuit

The targeted fault of the s-a-0 at the node \( e \) in the CUT is derived by inserting an \( L \) level logic signal to it at the simulation time 33 – 36 \( ns \). A simulation result of a faulty circuit is shown in Figure 8.

![Figure 7 Simulation time result of defect-free circuit](image)

Figure 8 Faulty circuit

In the faulty circuit result, \( e = 1 \) at the targeted simulation time. Even signals of 100 are generated by QPGn of the SA. It means that \( c = 1 \), \( b = 0 \), and \( a = 0 \). The targeted simulation time result is shown in Figure 9.

![Figure 8 Faulty circuit](image)

Figure 9. Simulation time result of faulty circuit

4. Conclusion

Stuck-at-faults occurring at input and output gates inside a combinational logic IC may be analyzed to be faster detected by a proposed signature analyzer of a BIST. The faults are a stuck-a-0 as well as a stuck-a-1.

References